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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANTONIO ASARO, BRIAN LEE,
KULDIP SHADRA, and GORDON CARUK

Appeal 2009-011544
Application 10/074,064
Technology Center 2100

Before GREGORY J. GONSALVES, JEFFREY S. SMITH, and JASON V. MORGAN, *Administrative Patent Judges*.

SMITH, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-28 and 33-35. Claims 29 and 32 have been canceled, and claims 30, 31, and 36 have been allowed. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

Invention

Appellants' invention relates to a configurable register method and structure including configuration logic to form a register value. A data bridge system, for connecting an interface of a computer system to a plurality of application-specific integrated circuits (ASIC), has a data bridge operatively coupled between the computer interface and the plurality of ASICs that employs the configurable registers. The data bridge has a read only memory for storing at least the initial values and mask values for each ASIC of the plurality of ASICs. The data bridge upon initialization forms base address registers and other configuration data that are queried by the computer system. The base address registers are thus programmable as a function of the initial values and mask values in the read only memory. Abstract.

Representative Claim

1. A data bridge system, comprising:

an interface for transferring data;

a plurality of application-specific integrated circuits (ASICs);

a data bridge operatively coupled to each: of the interface and the plurality of ASICs; and

the data bridge having a read only memory for storing at least initial values and mask values for each ASIC of the plurality of ASICs.

Examiner's Rejections[1]

Claims 1, 4-9, 19, 22, 23, and 25-27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gillespie (US 5,859,987), Surugucchi (US 6,094,699), and Venkat (US 5,857,083).

Claims 2, 3, 20, 21, 24, and 33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gillespie, Surugucchi, Venkat, and Appellants' admitted prior art.

Claims 10, 11, 13, 15-17, 34, and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gillespie, Surugucchi, Venkat, and Prabhu (US 6,675,292 B2).

Claims 14 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gillespie, Surugucchi, Venkat, Prabhu, and Appellants' admitted prior art.

Claim 28 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Prabhu and what is well known in the art.

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[1] Although the Examiner provides an analysis of claim 12 in light of the prior art on page 8 of the Examiner's Answer, the Examiner did not provide a statutory basis for rejecting claim 12 in the Final Rejection or the Examiner's Answer. Appellants also do not indicate a ground of rejection exists for claim 12 (App. Br. 16), and the Examiner agrees (Ans. 2). Therefore, we find that claim 12 has not been rejected by the Examiner.

PRINCIPAL ISSUES

Did the Examiner err in finding that the combination of Gillespie, Surugucchi, and Venkat teaches "initial values" and "mask values" stored in a read only memory within the meaning of claim 1?

Did the Examiner err in finding that configuring registers as read only as taught by Prabhu teaches "forming, from the initial values and the mask values, configurable registers, that upon initialization of a system cause the system to allocate resources to each of the plurality of ASICs" as recited in claim 10?

Did the Examiner err in finding that configuring registers as read only as taught by Prabhu teaches "at least one configurable register that includes register configuration logic and at least one register flop to contain an initial value and at least one mask flop that generates a mask bit for the configuration logic and wherein the register configuration logic configures the at least one register flop to be read and/or writable based on at least one mask value stored in the memory" as recited in claim 28?

ANALYSIS

Section 103 rejection of claims 1-9 and 19-27

Appellants contend that the "initial values" and "mask values" in the read only memory of claim 1 are not taught by Gillespie or Surugucchi. App. Br. 22. However, the "initial values" and "mask values" are a description of data that does not alter any method steps or structural limitations recited in claim 1. This non-functional descriptive material of claim 1 merely defines the meaning of the data stored in memory. Therefore, the "initial values" and "mask values" are non-functional

descriptive material that fail to distinguish the claim from the prior art in terms of patentability.

Appellants remaining arguments for claim 1 (App. Br. 20-22; Reply Br. 1-3) are directed to limitations not recited in claim 1 and are therefore not commensurate to the scope of claim 1.

We sustain the rejection of claim 1 under 35 U.S.C. § 103. Appellants have not presented arguments for separate patentability of claims 2-9 and 19-27, which thus fall with claim 1.

Section 103 rejection of claims 10, 11, 13-18, 33, and 35

Appellants contend that the cited references do not teach forming configurable registers from initial values and mask values, but instead refer to standard circuits that simply have register blocks where some of the registers are fabricated as either read only or read and write registers. App. Br. 23. The Examiner finds that Prabhu teaches forming a configurable register that includes register configuration logic, at least one register flop, and at least one mask flop. Ans. 6, citing Prabhu col. 5, ll. 41-56.

The cited section of Prabhu teaches designating registers as either general purpose registers or control and status registers. Although some control and status registers can be modified by program instructions, many registers can be configured as read only. However, the Examiner has not explained how the cited section of Prabhu teaches "forming, from the initial values and the mask values, configurable registers, that upon initialization of a system cause the system to allocate resources to each of the plurality of ASICs" as recited in claim 10.

We do not sustain the rejection of claim 10, and corresponding dependent claims 11, 13-18, 33, and 35, under 35 U.S.C. § 103.

Section 103 rejection of claim 28

Appellants contend that Prabhu does not teach mask flops that generate a mask bit for any configuration logic. Appellants also contend that Prabhu does not provide for any configuration logic that configures the register flop to be writeable as opposed to readable based on at least one mask value stored in memory. App. Br. 18-19. The Examiner finds that any register that is configurable as either read only or read/write would teach the limitations of claim 28. Ans. 10-11.

We do not agree with the Examiner. Claim 28 recites "at least one configurable register that includes register configuration logic and at least one register flop to contain an initial value and at least one mask flop that generates a mask bit for the configuration logic and wherein the register configuration logic configures the at least one register flop to be read and/or writable based on at least one mask value stored in the memory." The section of Prabhu cited by the Examiner merely teaches that registers can be configured as read only. Prabhu's teaching of registers that can be configured as read only does not teach the limitations of claim 28.

We do not sustain the rejection of claim 28 under 35 U.S.C. § 103.

Section 103 rejection of claim 34.

The Examiner finds that Prabhu teaches configurable registers. Ans. 7. However, claim 34 recites "at least one configurable register that includes register configuration logic and at least one register flop to contain an initial

value and at least one mask flop that generates a mask bit for the configuration logic and wherein the registered register configuration logic configures the at least one register flop to be read and/or writable based on at least one mask value stored in the memory."

The Examiner has not explained how the combination of Gillespie Surugucchi, Venkat, and Prabhu teaches the limitations of claim 34. We do not sustain the rejection of claim 34 under 35 U.S.C. § 103.

CONCLUSIONS OF LAW

The Examiner did not err in finding that the combination of Gillespie, Surugucchi, and Venkat teaches "initial values" and "mask values" stored in a read only memory within the meaning of claim 1.

The Examiner erred in finding that configuring registers as read only as taught by Prabhu teaches "forming, from the initial values and the mask values, configurable registers, that upon initialization of a system cause the system to allocate resources to each of the plurality of ASICs" as recited in claim 10.

The Examiner erred in finding that configuring registers as read only as taught by Prabhu teaches "at least one configurable register that includes register configuration logic and at least one register flop to contain an initial value and at least one mask flop that generates a mask bit for the configuration logic and wherein the register configuration logic configures the at least one register flop to be read and/or writable based on at least one mask value stored in the memory" as recited in claim 28.

DECISION

The rejection of claims 1, 4-9, 19, 22, 23, and 25-27 under 35 U.S.C. § 103(a) as being unpatentable over Gillespie, Surugucchi, and Venkat is affirmed.

The rejection of claims 2, 3, 20, 21, 24 and 33 under 35 U.S.C. § 103(a) as being unpatentable over Gillespie, Surugucchi, Venkat, and Appellants' admitted prior art is affirmed.

The rejection of claims 10, 11, 13, 15-17, 34, and 35 under 35 U.S.C. § 103(a) as being unpatentable over Gillespie, Surugucchi, Venkat, and Prabhu is reversed.

The rejection of claims 14 and 18 under 35 U.S.C. § 103(a) as being unpatentable over Gillespie, Surugucchi, Venkat, Prabhu, and Appellants' admitted prior art is reversed.

The rejection of claim 28 under 35 U.S.C. § 103(a) as being unpatentable over Prabhu and what is well known in the art is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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